Class-E_M Switching-Mode Tuned Power Amplifier—High Efficiency With Slow-Switching Transistor

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***Abstract*—In class-E switching-mode power amplifiers, the switch-current waveform includes a step change ("jump"), approximated by a ramp of $< 15\%$ of the period. At a transistor's highest useful frequency, the large input drive required for fast-enough switching yields marginal power gain. Objective: a high-efficiency power amplifier with jumpless current and voltage waveforms. Previously, that was proven impossible for amplifiers using only linear passive components and an ideal switch. We present the theory of a new topology that *does* achieve the objective: a class-E amplifier with *nonlinear* passive or active components in the load network. A "biharmonic" version was simulated, built, and tested. It comprises a main stage switching at the output frequency f_1, drawing dc power of approximately $3/4\,(P_{\mathrm{OUT\_RF}}/\mathrm{drain\_efficiency})$, and an auxiliary amplifier switching at $2f_1$, injecting $2f_1$-current into the circuit node at the main-stage transistor's output port to shape jumpless voltage and current waveforms. That switching (nonlinear) output port converts $2f_1$ power from the auxiliary amplifier to approximately 1/4 of the f_1 power at the load. Computer simulation, and measurement on a scaled-frequency 3.5-MHz prototype, show that switching losses practically disappear when the main-stage switch is operated in the jumpless regime.**

***Index Terms*—Amplifier, class E, class E_M, high efficiency, microwave, microwave power, power, power amplifier, RF, RF power, RF/microwave power, switching mode, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

THE class-E RF power amplifier [1]–[6] operates the output transistor as an on/off switch at the RF-output frequency; it is known as a good candidate when high efficiency is needed. Reference [3] contains a detailed overview of class-E amplifiers, including the conceptual "target" waveforms of switch voltage and current, and design equations for an amplifier using the published low-order lumped-elements load network that generates a first-order approximation to the "target" waveforms. The waveforms of switch voltage and current are generated by the transient response of the load network (the network external to the active part of the transistor; see Fig. 1) in response to the periodic operation of the on/off switch at the input port of the network. Higher order load networks generate closer approximations to the "target" waveforms shown in [1]–[3]. Reference [3] briefly discusses the realization of a class-E amplifier with transmission-line circuits instead of lumped-element components, and gives references to publications dealing with such transmission-line realizations. Example references for recent transmission-line class-E amplifiers are [7]–[10].

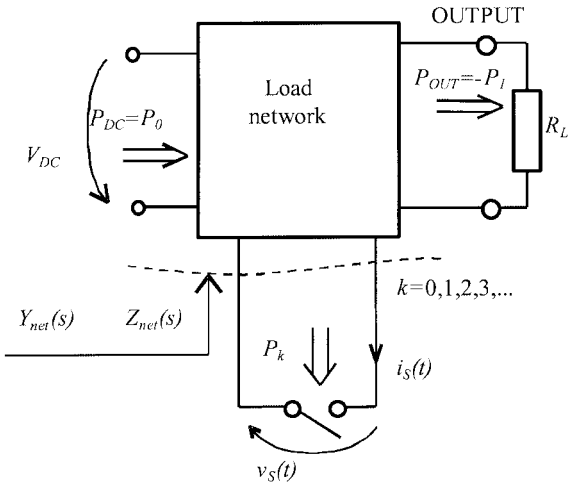

Fig. 1. Block diagram of a switching-mode power amplifier.

The class-E transistor has, in principle, a step-function ("jump") current turn-off. In an actual circuit, the current fall during turn-off is a ramp, ordinarily occupying 15% or less of the RF period. A basic limitation of the class-E amplifier at frequencies approaching the maximum usable frequency is that the efficiency declines with increasing values of the turn-off switching time because the switching power dissipation increases with increasing turn-off switching time (mathematical details below). The turn-off transition time is approximately inversely proportional to the square root of the input-drive power. The circuit performance becomes marginally acceptable at the frequency at which the input drive required for acceptable turn-off switching time results in marginally acceptable power gain and power-added efficiency (PAE).

This paper addresses efficiency improvement in class-E amplifiers operating at frequencies near what had previously been the maximum usable frequency discussed above. The efficiency, power gain, and PAE are increased by shaping the

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voltage waveform differently to allow slow switching without the attendant loss of efficiency. We begin by analyzing the action during the transistor's turn-off transition in the published circuit of [1]–[4]. At switch turn-off, the switch current falls linearly from a nonzero value to zero in a time as short as can conveniently be obtained with an acceptable amount of input-drive power. The resulting collector or drain efficiency is

$$\eta = 1 - \frac{1}{12}\theta_s^2 \tag{1}$$

where θ_s is the turn-off-switching transition angle in radians.[1] Numerical evaluation of (1) shows that high efficiency can be achieved even if the turn-off switching time is an appreciable fraction of the period: e.g., for the power losses due to nonzero turn-off switching time, the efficiency (100% at zero switching time) ranges from 96.7% to 86.8% for switching times from 10% to 20% of the period. (Other sources of power dissipation reduce the efficiency further, but here we are concerned with only the effects of switching time.) The power transistor's switching time is approximately $K/\sqrt{P_{\rm drive}}$, where K is a constant for a particular transistor and $P_{\rm drive}$ is the input-drive power to that transistor. A large K corresponds to a slow switching time (associated with low f_T for a bipolar junction transistor or high $C_{\rm iss}$ for an FET) and, hence, a low value of efficiency from (1).

However, a slow-switching transistor *further* degrades the *overall* efficiency because the switching operation requires a *driver stage* whose power consumption: 1) decreases the overall efficiency and 2) is proportional to the output-transistor's K value, i.e., more input drive (hence, more power consumption) is needed with a slower switching output transistor. Equipment users are interested mainly in the PAE of the system

$$\text{PAE} = \frac{P_{\text{out RF}} - P_{\text{in RF to first stage if from external source}}}{P_{\text{in DC to all stages}}}. \tag{2}$$

The present authors, like the authors of [1] and [2], wanted to find a way to make the circuit work well *without* requiring a jump in the switch-current waveform at turn-off so as to allow efficient operation at frequencies high enough that the switch turn-off transition would occupy a substantial fraction of the waveform period, e.g., 30% or more. Unfortunately, [11] showed that the class-E amplifier can deliver nonzero output power only if at least one of the switch waveforms (either voltage or current) has a jump (as seen in the current waveforms of [1, Fig. 4(e)], [2, Fig. 4B], and [3, Fig. 3]) under the assumption that the circuit comprises an ideal switch and linear passive components. The conclusions of [11] were confirmed in [12] and [13]. Reference [14] investigates: 1) the possibility of achieving nonzero output power with jumpless switch voltage *and* current waveforms in a circuit comprising an ideal switch and *nonlinear* passive components and 2) the effects on the switch-voltage and switch-current waveforms and the resulting amplifier efficiency of harmonic-current injection into the network from an external source. Reference [14] does not show clearly which topologies can simultaneously yield a jumpless voltage waveform and a jumpless current waveform. That omission is remedied in this paper.

If a method such as that in [14] could, in fact, be implemented so that *both* the voltage and current waveforms could be jumpless, then the circuit could tolerate slow switching times with less loss of efficiency than is shown in (1), and a transistor with a given switching speed could provide higher efficiency versus frequency in such a circuit than when that transistor is used in the classical class-E circuit of [1]–[3] (provided that the conduction losses do not increase by more than the switching losses decrease). In addition, the driver-stage output and input powers could be reduced, further increasing the overall efficiency, because fast switching speed of the output transistor would now be less important, so lower input drive to the output transistor would be acceptable.[2] In most cases, the current switching time is proportional to the current to be switched, and inversely proportional to the input-drive voltage (for FETs) or current (for bipolar junction transistors), and operation with a *jumpless* switch-current waveform yields a greatly reduced switching transition time and its associated switching losses.

In this paper, we describe an implementation having jumpless switch-voltage and switch-current waveforms; we call it "class E_M"; the subscript "M" indicates "microwave," the frequency region in which the jumpless-waveform properties of this amplifier are expected to be most useful. The lowest order ("biharmonic") implementation of the class-E_M principle comprises the following two-part output stage:

- main amplifier that consumes dc power equal to approximately 3/4 of the load power, and converts this power and the power generated by the auxiliary amplifier to power at the output frequency f_1;
- smaller auxiliary amplifier (or a varactor frequency-multiplier), phase-locked to the main amplifier, which generates approximately 1/4 of the load power at the frequency $2f_1$.

[1]For the derivation of (1) see [1, eq. (8)] for η_c. Simplify the parameter A, defined in the line below (5), to unity by assuming infinite Q_L (network loaded Q) and, therefore, a pure-sine current in *L2–C2*. Drop the term involving $V_{\rm CE(sat)}$ because here we are concerned with the effects of only switching time. Apply the approximation that $1/(1+x) \approx (1-x)$ if $x \ll 1$. The result is identical with (1).

[2]The theoretical analysis presented in this paper assumes infinitely short turn-on and turn-off switching times because this greatly simplifies the analysis, while still being a good approximation to the operation of an actual class-E_M circuit. *Turn-off switching* begins when the switch current (determined by the external "current-source" circuit) *already is at or is very close to zero and varies slowly due to the approximately zero value of its time derivative*. Then, even with small input drive, the time for the current to fall to zero (if it is not *already* at zero) is very short, in contrast to the turn-off switching in the original class-E circuit, in which the current must jump to zero from 70% of the peak current. Hence, a given transistor will show faster turn-off switching in a class-E_M circuit than in a class-E circuit, even with small input drive. That makes the class-E_M amplifier suitable for operation at frequencies higher than can be accommodated by the same transistor in class-E operation. The *turn-on switching* conditions are similar in class-E_M and class-E operation: The current increases slowly from zero, at a well-defined rate. The switch remains voltage-saturated if it can support the well-defined di/dt. In actual practice, that is an easy condition to meet, and small input drive is sufficient. Much experimental operation and simulation (which shows details not easily visible experimentally) of the class-E amplifier have shown that power dissipation during the turn-on switching is negligibly small in relation to other power losses, e.g., by two orders of magnitude. Since the turn-on switching conditions are similar in the class-E_M circuit, the authors expect the same low turn-on switching loss, even with small input drive, as has already been seen in extensive experience with the class-E circuit. Conduction: In both E_M and E, the input drive must be sufficient to keep the transistor in voltage saturation during the conduction interval (after the turn-on switching and before the turn-off switching), when it is carrying substantial current, but with low di/dt.

The main amplifier has jumpless switch-current and switch-voltage waveforms, while the auxiliary amplifier can be a usual switching-mode amplifier (e.g., class E). (If the frequency multiplier is fed from the output of the main amplifier, the load power is reduced by the amount of power converted by the frequency multiplier from frequency f_1 to frequency $2f_1$ to change the waveform shapes to continuous ones as shown later in the paper.) Higher order implementations can use harmonics of order higher than two or multiple harmonics ("polyharmonic" implementation). The higher order implementations will have different distributions of the total power between the two (or more for polyharmonic) parts of the amplifier than the "$3/4 + 1/4$" shown for the biharmonic implementation using f_1 and $2f_1$. (We are not aware of any net advantage to be gained from using harmonics higher than $2f_1$; a disadvantage is that the power gain and efficiency of the auxiliary amplifier decrease at harmonic frequencies higher than $2f_1$.)

Section II deals with the general mathematical theory of the new family of amplifiers that can operate with jumpless voltage and current waveforms. Section III deals with the consequences of the basic equations derived in Section II. Section IV deals with the waveforms in the lowest order ("biharmonic") member of the new family. Section V gives the detailed design, simulation, and experimental verification of a biharmonic class-$\mathrm{E_M}$ amplifier operated at a scaled frequency of 3.5 MHz, and the reasons for making the measurements at 3.5 MHz. The measured PAE of the slow-switching continuous-waveforms main stage was 85.2% at 13.2-W output. Section V also reports simulations combined with efficiency estimations of class-$\mathrm{E_M}$ and class-E amplifiers operating at 870 MHz, 3.2-W output, and a comparison between those two amplifiers. Section VI summarizes the new results. Section VII discusses practical questions that need further study. The relationship between class $E/\mathrm{E_M}$ (operating the transistor in switching mode) and classes F [15]/HCA [16], [17] (operating the transistor in current-source mode) is discussed in Section VIII.

II. General Power Equations of an Ideal Switch in an Amplifier Operating in the Lossless Mode

To lay the mathematical foundation for the genesis of the circuit to be described in Section IV, this section reviews the general power equations (15) and (16) below (related to [11, eqs. (10)–(14)], [12, eqs. (13) and (21)], and [14, eq. (17)]), that characterize the interaction of an ideal switch with a linear or nonlinear network, in an amplifier operating in the lossless mode. Here and in Section III, we add further considerations not in the previous publications, regarding the generic circuit topologies of Fig. 2 and the relations among the parameters of the switch-voltage and switch-current waveforms shown in Fig. 3.

Fig. 1 shows the block diagram of a switching-mode power amplifier. The switch is connected across one port of a linear or nonlinear network called the "load network." Whether the network is linear or nonlinear, it can be taken as linear during the infinitely short switch transitions. We assume that the network is *a lumped-element network*; thus the impedance Z_{net} seen by the switch during a switching transition can be characterized in the frequency domain by a rational function (3) with m poles

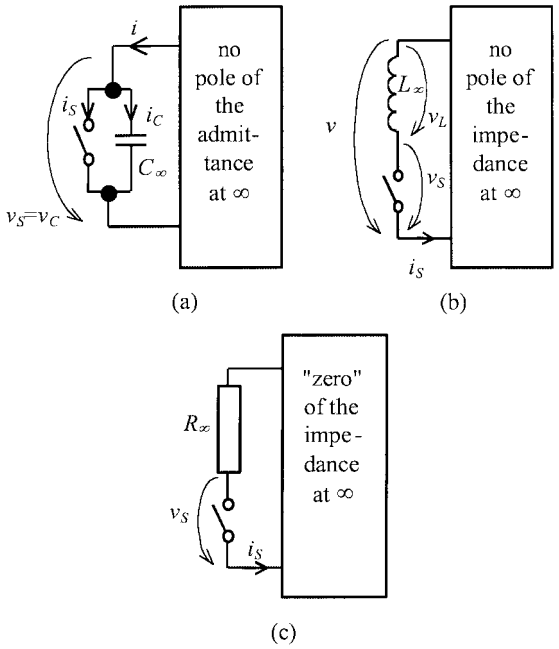

Fig. 2. Element extraction from a linear switch-driven network. Virtual circuit topologies. (a) Switch with shunt capacitance. (b) Switch with series inductance. (c) Switch with series resistance.

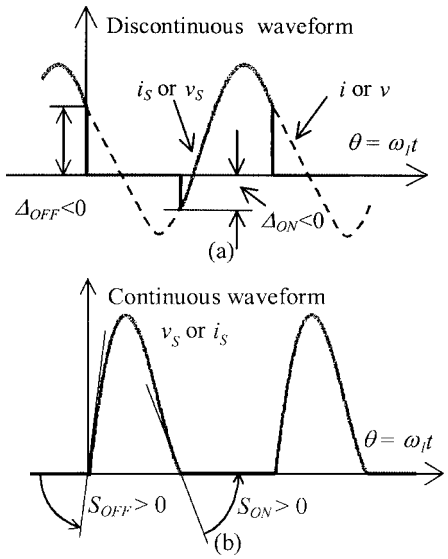

Fig. 3. Possible switch waveforms of a switching-mode power amplifier. (a) Discontinuous waveform. (b) Continuous waveform. S is the jump of the slope of the continuous waveform in (b).

and n zeros. From stability considerations, $(m-n) = -1, 0,$ or $+1$. Thus,

$$Z_{\mathrm{net}}(s) = \frac{\sum_{i=0}^{n} A_i s^i}{\sum_{i=0}^{m} B_i s^i}, \qquad \text{where } B_m > 0 \text{ and } A_n > 0. \quad (3)$$

The impedance $Z_{\mathrm{net}}(s)$ or admittance $Y_{\mathrm{net}}(s)$ can be written as

$$\left.\begin{aligned} Y_{\mathrm{net}}(s) &= C_\infty \cdot s + Y_r(s) \\ Z_{\mathrm{net}}(s) &= L_\infty \cdot s + Z_r(s) \\ Z_{\mathrm{net}}(s) &= R_\infty + Z_r(s) \end{aligned}\right\}$$

where

$$\frac{A_n}{B_m} = \begin{cases} C_\infty^{-1}, & \text{if } m = n+1 \\ L_\infty, & \text{if } m = n-1 \\ R_\infty, & \text{if } m = n. \end{cases} \tag{4}$$

The decomposition in (4) means that, depending on the topology of the load network, a capacitance C_∞, an inductance L_∞, or a resistance R_∞ can be extracted from (3). Fig. 2 shows the three possible topologies of the switch and its embedding network. The extracted parameters characterize the high-frequency behavior of the impedance at the considered switching moment. In most practical cases, the extracted elements shown in Fig. 2 can be identified with actual circuit elements of the switching-mode amplifier (for example, in a classical class-E amplifier [1]–[3], C_∞ is the inherent output capacitance of the transistor switch plus the external shunt capacitance (if any) connected across the switch).

We are interested in power components at harmonic frequencies flowing into the switch (see Fig. 1). (The power at a particular harmonic can be negative, indicating that the power at that harmonic frequency is coming from the switch.) Let the power flowing into the switch at the kth harmonic be denoted by P_k.

In order to achieve 100% power-conversion efficiency (no power dissipation in the switch or in the network), the switch must be operated so that

$$\sum_{k=0}^{\infty} P_k = 0. \tag{5}$$

Equation (5) can be satisfied if the load network is tuned so that the voltage on C_∞ is zero at the switch turn-on [for the topology in Fig. 2(a)] or the current through L_∞ is zero at the switch turn-off [for the topology in Fig. 2(b)]. The topology in Fig. 2(c) does not need such constraints on the waveforms, but this topology is not well suited for a high-efficiency amplifier because the resistor in series with the switch causes unwanted power dissipation unless its resistance is negligibly small. If the resistance is negligibly small, the circuit becomes the circuit of Fig. 2(a) or (b).

In the subsequent analysis, therefore, we focus on only the topologies of Fig. 2(a) and (b), which are duals of each other.[3] We assume that the switch is ideal and operates without loss so that (5) is satisfied. Fig. 3 shows possible switch waveforms. The current waveform may have jumps (Δ_{ON} or Δ_{OFF}) in the circuit of Fig. 2(a), and the voltage waveform may have jumps in the circuit of Fig. 2(b). As shown in Fig. 3(b), the complementary waveforms (voltage and current, respectively) are continuous (without jumps), but their slopes can have jumps. We measure the waveform slope S in volts per radian or amperes per radian, depending on whether the voltage waveform or the current waveform is the continuous one.

[3]The topology of Fig. 2(b) is included for mathematical completeness. However, as of 2003, the output capacitance of all transistors commonly used at frequencies above approximately 10 MHz is large enough that the output capacitance itself becomes C_∞ (or a substantial part of C_∞ when augmented by an intentional external capacitor). That makes the circuit correspond to the topology of Fig. 2(a). The topology of Fig. 2(b) can be achieved at lower frequencies, but the class-E_M technique described here is not needed at such low frequencies.

Denoting $\omega_1 = 2\pi f_1$, the angular velocity of the fundamental frequency of the waveforms (taken as periodic), a proportionality relation between S and Δ can be written as

$$\begin{cases} S_V = -\dfrac{\Delta_I}{\omega_1 C_\infty}, & \text{for the circuit of Fig. 2(a)} \\ S_I = -\dfrac{\Delta_V}{\omega_1 L_\infty}, & \text{for the circuit of Fig. 2(b).} \end{cases} \tag{6}$$

Subscripts I and V in (6) indicate current and voltage, respectively.

In the following paragraphs, we show the main steps of the derivation of a general equation (15) that we shall use later in this paper. Readers who are not concerned about the mathematical details can jump from here to (15). The derivation is shown for the topology in Fig. 2(a), but a similar derivation accommodates the dual topology in Fig. 2(b). The presentation uses elements of derivations in [11], [12], and [14], but unlike those publications, the derivation below avoids using concepts from the mathematical theory of distributions.

We use [11, eq. (10)] or [12, eq. (13)], which can be written, in our notation, as

$$\sum_{k=1}^{\infty} k^2 P_k = \frac{1}{T\omega_1^2} \int_0^T v_S' i_S' dt. \tag{7}$$

Here, $T = 2\pi/\omega_1$ is the period of the periodic waveforms, v_S' and i_S' are time derivatives of the switch voltage and switch current, and P_k is the kth harmonic power flowing into the switch. (For the origin of (7), author Telegdy will be glad to send a more-detailed description on request.)

The definite integral in (7) can be calculated by dividing the integration interval into two or more sub-intervals, each of which begins and ends at a switching transition, and summing the sub-integrals.

Consider now a switching-transition interval centered at the moment $t = t_0$, with duration $2\Delta t$. $v_S' i_S'$ is zero before and after the switching, but can be nonzero during the switching interval.

The basic assumption of the derivation is that the switching transition is fast enough that the part of the system that remains after the extraction of C_∞ [see Fig. 2(a)] cannot change its state during the switching transition. This condition is met if the switching transitions are infinitely short, i.e., $\Delta t \to 0$. Thus,

$$I_0 = i_S(t) + i_C(t) = \text{constant} \tag{8}$$

where i_S, i_C, and i are defined in Fig. 2(a). Taking the time derivative of (8) gives

$$i_S'(t) = -i_C'(t). \tag{9}$$

The current jump at a switching moment is

$$\Delta_I = \begin{cases} +i(t_0) = i_C(t_0 - \Delta t) & \text{for turn-on} \\ -i(t_0) = i_C(t_0 + \Delta t) & \text{for turn-off} \end{cases} \tag{10}$$

where subscript I and subscript V used later indicate the switching moment for current and voltage, respectively. The proportionality factor between the current and time derivative

of the voltage is the reciprocal of C_∞. Considering also that C_∞ is connected across the switch, we can write

$$v'_S(t) = v'_C(t) = \frac{1}{C_\infty} i_C(t). \tag{11}$$

(If C_∞ is nonlinear, its value should be taken as the value at zero voltage. Since the voltage on C_∞ cannot change during the infinitely short switching transition, a nonlinear C_∞ can be taken as constant during that switching interval.) Substituting (9) and (11) into the integral in (7), we can write

$$\begin{aligned}\int_{t_0-\Delta t}^{t_0+\Delta t} i'_S(t)\cdot v'_S(t)dt &= -\int_{t_0-\Delta t}^{t_0+\Delta t} i'_C(t)\cdot\frac{i_C(t)}{C_\infty}dt \\ &= -\frac{1}{2C_\infty}\left[i_C^2(t_0+\Delta t) - i_C^2(t_0-\Delta t)\right].\end{aligned} \tag{12}$$

Since

$$\begin{cases} i_C(t_0+\Delta t) = 0 \text{ for turn-on} \\ i_C(t_0-\Delta t) = 0 \text{ for turn-off} \end{cases} \tag{13}$$

and taking into account (10),

$$\int_{t_0-\Delta t}^{t_0+\Delta t} i'_S(t)\cdot v'_S(t)dt = \begin{cases} +\dfrac{1}{2C_\infty}\Delta_I^2 \text{ for turn-on} \\ -\dfrac{1}{2C_\infty}\Delta_I^2 \text{ for turn-off.} \end{cases} \tag{14}$$

Using (6), we turn to using S_V in place of one of the factors Δ_I in Δ_I^2 and we then substitute (14) into (7). After rearranging the result, the final equation (15) results by summing all of the integrals of type (12) corresponding to turn-on transitions and (separately) turn-off transitions (Note that the voltage-slope jumps are measured in units of volts per radian.)

$$\begin{aligned}&\sum_{k=1}^{\infty} k^2 P_k \\ &= \frac{1}{4\pi}\left(\sum_{\substack{\text{all turn-off}\\ \text{transitions}\\ \text{in a cycle}}} S_{\text{OFF}}\Delta_{\text{OFF}} - \sum_{\substack{\text{all turn-on}\\ \text{transitions}\\ \text{in a cycle}}} S_{\text{ON}}\Delta_{\text{ON}}\right).\end{aligned} \tag{15}$$

(To simplify the notation, we have omitted indexes in the sum (indicating different switching moments), and subscripts V and I.) Equation (15) holds if the switching transitions are fast (i.e., (8) is valid), no matter how the switch current varies with time during the switching transitions.

Equation (15) is a general equation for harmonic powers flowing in a switch from the linear or nonlinear load network of an amplifier of the topology shown in Fig. 2(a) or (b) operating in the lossless mode. Other forms of (15) can be obtained by substituting S or Δ from (6) into (15). In the circuit of Fig. 2(a), the switch is turned "on" when the capacitor voltage v_C is zero; in the circuit of Fig. 2(b), the switch is turned "off" when the inductor current i_S is zero. The switch carries a current waveform $i_S(t)$ and sustains a voltage waveform $v_S(t)$. In order to achieve high efficiency, a lossless load network is needed, i.e., the load network can include any types of components *except* resistors. (Parasitic resistances in real components reduce the efficiency from the ideal 100%.) If, in addition, the load network is linear (as is usually the case), the harmonic power of the switch is conserved). Thus, (15) is valid as the general equation for the power flow at all harmonic frequencies: 1) in an ideal switch connected to a linear or nonlinear network and 2) in a *linear* network driven by an ideal switch; in both cases 1) and 2), for the amplifier operating in the lossless mode. Unless stated otherwise, the load network is considered to be linear, for the subsequent discussions.

As stated in Section I, jumpless-waveform operation is desired whenever the operating frequency is so high that the switch turn-off transition time cannot easily be made a small fraction (e.g., $< 20\%$) of the period. In jumpless operation, S and Δ are zero in both of the sums in (15). Thus, a new general equation can be written for power amplifiers comprising a linear or nonlinear network driven by an ideal switch, and operating in the lossless mode with jumpless voltage and/or current waveforms ("and" if the network is nonlinear, or is linear and has harmonic power injected into it, as shown later in Fig. 4, or if the network is linear)

$$\sum_{k=1}^{\infty} k^2 P_k = 0. \tag{16}$$

If the load network is linear and lossless, P_k can be harmonic powers: 1) flowing in the switch and/or 2) flowing in the load network via ports other than the switch-connection port. In case 1), the total power P_k at the kth harmonic is the summation of the kth harmonic powers at all of the ports, except the switch-connection port.

III. Consequences of the General Equations (15) and (16)

To show the consequences of the general equation (15), using the simplest mathematical formulation, suppose that there is positive power flowing into the switch at dc and positive power flowing out of the switch at the switching frequency; and, suppose further, for this simple illustration (but not in general), the load network is linear, is tuned to a specific frequency slightly below the switching frequency [1]–[3], and includes a dc block and a harmonics-rejection filter before the load resistance. The voltage and current waveforms at the load can then be taken as pure sinusoids at the switching frequency and all of the power delivered to the load is at only the switching frequency. With those assumptions,

$$\left.\begin{aligned} &P_0 = P_{\text{DC}} \\ &P_1 = -P_{\text{OUT}} \\ &P_i \to 0 \text{ for } i = 2,3,\ldots \end{aligned}\right\}. \tag{17}$$

Substituting (17) into the basic (15), we obtain, for this example,

$$\begin{aligned} P_{\text{OUT}} &= -\frac{1}{4\pi} S\cdot\Delta \\ &= \begin{cases} -\dfrac{\omega_1 C_\infty}{4\pi} S_V^2 = -\dfrac{1}{4\pi\cdot\omega_1 C_\infty}\Delta_I^2 \text{ for Fig. 2(a)} \\ -\dfrac{\omega_1 L_\infty}{4\pi} S_I^2 = -\dfrac{1}{4\pi\cdot\omega_1 L_\infty}\Delta_V^2 \text{ for Fig. 2(b).} \end{cases} \end{aligned} \tag{18}$$

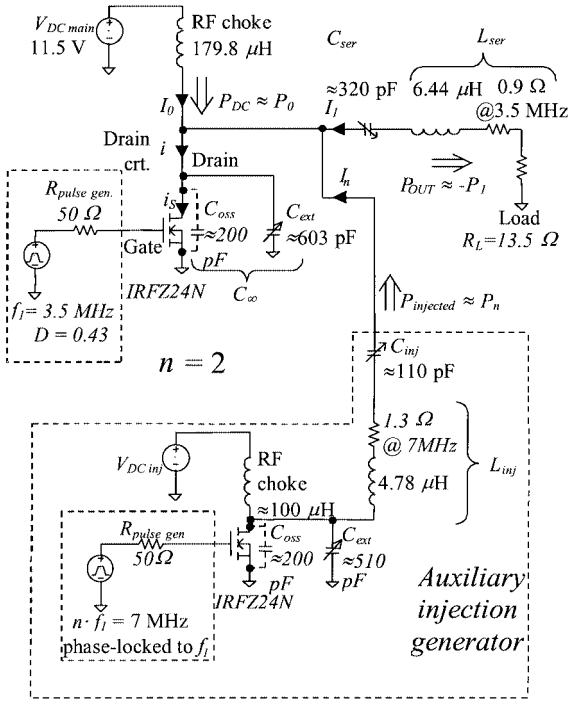

Fig. 4. Schematic of a 3.5-MHz 13.2-W class-E_M amplifier built and tested.

In this illustrative case, we can conclude that the output power is uniquely determined by: 1) the waveform jump on the switch (current or voltage) and 2) the infinite-frequency behavior of the network seen by the switch (i.e., the shunt capacitance C_∞ or the series inductance L_∞). No power can be generated with a switch connected to a linear load network if both the switch voltage and switch current are jumpless and all non-dc power flowing through the load network is at only one frequency.

In order to satisfy both of the requirements of 1), jumpless voltage and current waveforms on the switch, and 2) nearly pure sinusoidal output waveform with nonzero output power, *we must allow power flow in the system at two or more harmonically related frequencies*. This can be done in either of two ways: 1) by using *nonlinear* elements in the load network to convert fundamental-frequency power to a desired harmonic frequency or 2) by injecting the harmonic-frequency power into the network from an external source, such as the "Auxiliary injection generator" amplifier in Fig. 4. In the case of using nonlinear elements, those elements should be reactive (i.e., nondissipative), such as varactors, in order to achieve high efficiency. Amplifiers achieving continuous waveforms by using principle 1) or 2) are considered as a new type of amplifiers called "class E_M."

For the next step, consider the following example, which we call the "biharmonic" case: 1) the power flowing into the switch is nonzero at dc, at the fundamental frequency f_1, and at one harmonic of the fundamental (let us say the nth harmonic) and 2) the switch voltage *and* current waveforms are *both* jumpless as follows:

$$\begin{cases} P_0 \neq 0, P_1 \neq 0, P_n \neq 0, & n \geq 2 \\ P_k = 0, & \text{for } k \neq 0, 1, \text{ or } n. \end{cases} \tag{19}$$

For the variant with a linear lossless load network and nth harmonic external harmonic injection, we can write

$$\left.\begin{aligned} P_0 &= P_{\mathrm{DC}} \\ P_1 &= -P_{\mathrm{OUT}} \\ P_n &= P_{\mathrm{injected}} \end{aligned}\right\}. \tag{20}$$

For the variant with a lossless nonlinear frequency multiplier, the power injected into the main stage (i.e., P_{injected}) is still present in the circuit. This power component is produced by the multiplier that consumes an equal amount of power at the fundamental frequency. Thus, the equations are

$$\left.\begin{aligned} P_0 &= P_{\mathrm{DC}} \\ P_1 &= -P_{\mathrm{OUT}} - P_{\mathrm{multiplier\ input}} \\ P_{\mathrm{injected}} &= P_n = P_{\mathrm{multiplier\ input}} \end{aligned}\right\}. \tag{21}$$

Applying the general equation (16) for the "jumpless switch voltage *and* current" version of the circuit of Fig. 2(a) or (b) yields

$$\sum_{k=1}^{\infty} k^2 P_k = P_1 + n^2 P_n = 0. \tag{22}$$

Therefore,

$$P_n = -\frac{1}{n^2} P_1. \tag{23}$$

Equation (16) and its particular case (23) represent necessary power conditions for achieving jumpless switch voltage *and* current waveforms in the example biharmonic case.

Taking into account the total power balance (5) of the switch, the dc power flowing into the switch is

$$P_0 = -P_1 \left(1 - \frac{1}{n^2}\right). \tag{24}$$

In the variant with a varactor frequency multiplier (if that is used instead of an auxiliary harmonic-frequency amplifier), the multiplier takes a part of the active power from the switch at the fundamental frequency, and delivers it back to the load network at the nth harmonic frequency. As (16) is a *necessary* condition, but not a *sufficient* one, it does not by itself guarantee lossless operation. In both variants, the harmonic components of the current injected into the load network must also satisfy defined phase and amplitude conditions in order to achieve jumpless switch voltage *and* current waveforms and amplifier operation in the lossless mode. The analysis presented in Section IV shows that these required phase and amplitude conditions can be derived analytically. Numerical solutions yield explicit design requirements for *a priori* circuit designs.

The harmonic-power generator must be phase-locked to the main class-E_M stage to ensure that the phase of the injected harmonic-frequency current remains at the proper value, relative to that of the fundamental in the main amplifier circuit. For operation at frequencies near the upper limit of the transistor's switching-time capabilities, the biharmonic amplifier can be energetically superior to a "classical" class-E amplifier [1]–[3] using the same power transistor and supplying the same output power at the same operating frequency. That is because

the biharmonic amplifier can tolerate slow transistor turn-off with much less loss of efficiency than in the classical class-E amplifier. In addition, less input drive is needed for the biharmonic amplifier because slower switching times are tolerable (the switching times are inversely proportional to the square root of the input-drive power) and switching times are decreased due to jumpless waveforms. The power consumption of the driver stage is then lower, and the PAE is higher. (The minimum required input drive is that needed to operate the transistor in deep-enough voltage saturation while conducting substantial current so as to result in a low-enough conduction power dissipation.) These considerations set a lower bound on the efficiency of the harmonic-frequency power generator to be able to achieve higher overall efficiency than with the classical class-E circuit.

IV. Theoretical Waveforms of Biharmonic Class-E Amplifiers

To derive the waveforms of the main stage of the biharmonic class-E (class-E_M), amplifier of Fig. 4, we can assume that the resultant current of the switch and its parallel capacitor contains only dc, fundamental, and nth harmonic terms (to the best of our knowledge, $n = 2$ is the best choice, but the analysis here is general and allows using any value of n)

$$i = I_0 + I_{1A}\cos\theta + I_{1B}\sin\theta + I_{nA}\cos n\theta + I_{nB}\sin n\theta \quad (25)$$

where $\theta = 2\pi f_1 t$ is the "angular time" and f_1 is the fundamental frequency of the waveforms. This is a good approximation if the loaded quality factors of the output circuit and injection circuit are high and the inductance of the RF choke is also high. We assume that the switch in the main amplifier operates at the fundamental frequency f_1. Taking into account the topology of the amplifier (Fig. 4), it can be seen that the theoretical parameter C_∞ in Fig. 2(a) is equal to the parallel shunt capacitance of the switch $C_\infty = C_{\text{ext}} + C_{\text{oss}}$.

The voltage of the switch during the "off" interval (begins at $\theta = 0$ and ends at $\theta = \Gamma$) can be calculated by taking the definite integral of the current in C_∞. Using θ as an integration variable, the voltage can be written as

$$v_S(\theta) = \frac{1}{2\pi f_1 C_\infty}\int_0^\theta i(\theta)d\theta, \qquad \text{for } \theta \le \Gamma. \quad (26)$$

The conditions for optimum operation (with jumpless waveforms and unipolar switch current) are

$$\left.\begin{array}{l} i(\theta = 0) = 0 \\ i(\theta = \Gamma) = 0 \\ v(\theta = \Gamma) = 0 \\ \dfrac{d}{d\theta} i(\theta)\,|_{\theta=0} = 0 \end{array}\right\}. \quad (27)$$

By evaluating the integral (26) using the equation for current (25) and substituting the result into (27), after grouping the similar terms together (author Telegdy will be glad to send a more-detailed derivation on request), a linear equation system results, which can be represented in matrix form as

$$\begin{pmatrix} 1 & 0 & 1 & 0 \\ \cos\Gamma & \sin\Gamma & \cos n\Gamma & \sin n\Gamma \\ 0 & 1 & 0 & n \\ \sin\Gamma & 1-\cos\Gamma & \dfrac{1}{n}\sin n\Gamma & \dfrac{1}{n}(1-\cos n\Gamma) \end{pmatrix} \times \begin{pmatrix} I_{1A} \\ I_{1B} \\ I_{nA} \\ I_{nB} \end{pmatrix} = \begin{pmatrix} -I_0 \\ -I_0 \\ 0 \\ -I_0 \end{pmatrix}. \quad (28)$$

One can calculate the switch voltage and current waveforms of the new class-E_M amplifier by solving (28) (valid at any switch duty ratio) and calculating (26) for the switch voltage and (25) for current.[4] In particular, for 50% duty ratio (i.e., $\Gamma = \pi$) and $n = 2$ (meaning that the harmonic frequency used is $2f_1$), solution of (28) yields the following values for current components:

$$\begin{aligned} I_{1B} &= -\frac{\pi}{2} I_0 \\ I_{1A} &= 0 \\ I_{2B} &= \frac{\pi}{4} I_0 \\ I_{2A} &= -I_0. \end{aligned} \quad (29)$$

Equations for switch current and voltage can be written as

$$i(\theta) = I_0\left[1 - \frac{\pi}{2}\sin(\theta) + \frac{\pi}{4}\sin(2\theta) - \cos(2\theta)\right] \quad (30)$$

for $\theta = \pi$ to 2π and

$$v_S(\theta) = \frac{I_0}{16\pi f_1 C_\infty} \times \left[8\theta + 4\pi\cos(\theta) - \pi\cos(2\theta) - 4\sin(2\theta) - 3\pi\right] \quad (31)$$

for $\theta = 0$ to π

Fig. 5(b) shows waveforms (30) and (31) graphically.

Solutions for third-order harmonic injection and 33% duty ratio can be seen in Fig. 5(c). Having determined the waveforms on the switch (with chosen values of Γ and n), two impedances useful for circuit design can be computed: 1) the input impedance at $2f_1$ at the switch-connection port (seen as a load by the Auxiliary injection generator) and 2) the impedance $Z_{\text{net}}(s)$ at f_1 of the input port of the load network, which is driven by the switch. As we assumed high loaded Q for the load network and a high-inductance high-Q RF choke, impedance 2) is practically equal to C_∞ shunted by the series-connected

[4]With certain combinations of parameters (e.g., $\Gamma = \pi$ and $n = 3$) (28) cannot be solved, thus, these combinations cannot be used in practice. In addition, there exist parameter combinations (e.g., $\Gamma = \pi$ and $n = 4$) that do yield a solution for (28), but the resulting switch voltage takes negative values for some time interval during the OFF state. These cases are also to be avoided, unless the switching element can withstand negative voltages, possibly with the addition of an antiparallel diode connected across the switch. If the antiparallel diode turns on during the OFF state of the switch, the circuit can still work well, but the equation system (28) is no longer valid so other means must be used to predict the circuit operation.

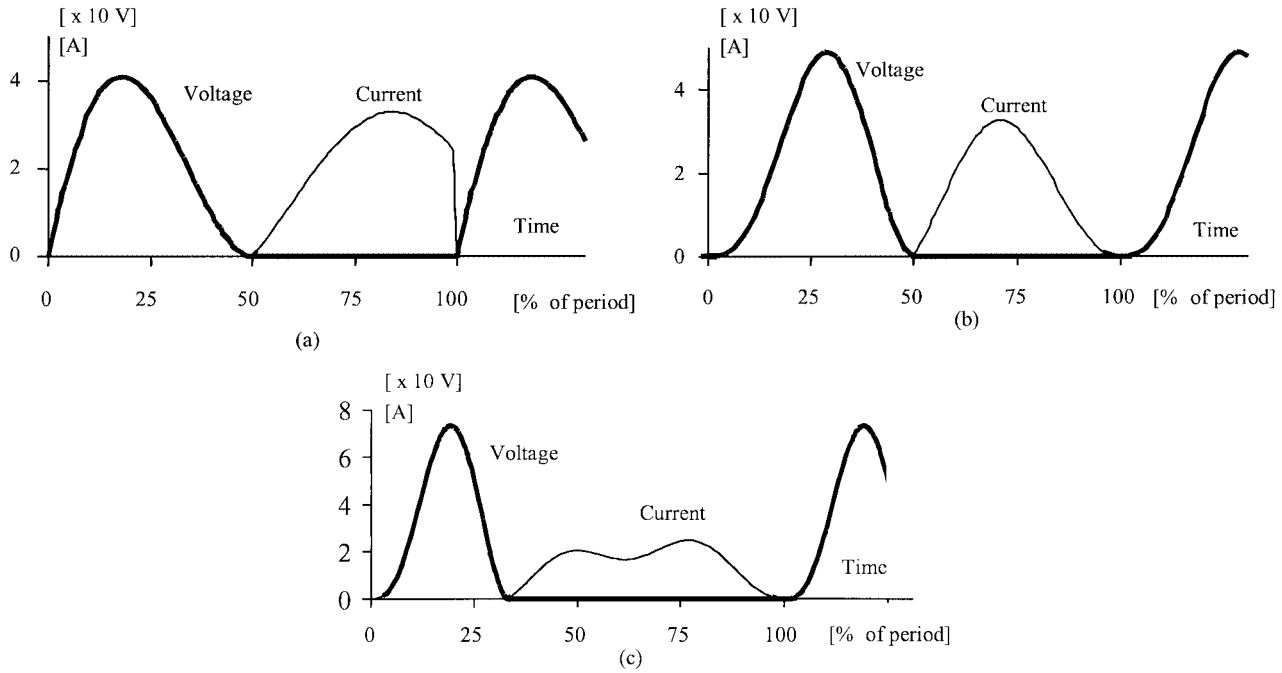

Fig. 5. Theoretical switch waveforms of a class-E and biharmonic class-E_M amplifier with dc power supply 11.47 V and output power $(12.34 + 0.82)$ W. (a) Class-E amplifier. (b) Class-E_M amplifier (main stage) with second-harmonic power injection ($n = 2$ and duty ratio 50%). (c) Class-E_M amplifier (main stage) with third-harmonic power injection ($n = 3$ and duty ratio 33%).

string of $C_{\rm ser}$, $L_{\rm ser}$, and the load R_L (see topology in Fig. 4). Separate sub-parts of those impedances can also be computed, omitting chosen components, e.g., omitting C_∞ of impedance 2) for the case in which C_∞ is already provided by the output capacitance of the switch, and the designer wants to know the impedance to be provided by the series combination of $C_{\rm ser}$, $L_{\rm ser}$, and R_L. The preceding impedances 1) and 2) can be determined by Fourier-series analyses of the waveforms of switch voltage and switch current, knowing the value of C_∞. The waveforms of the auxiliary amplifier (or frequency multiplier) are the usual waveforms known from the literature. Table I shows the main equations for the theoretical parameters.

TABLE I
THEORETICAL CIRCUIT ELEMENTS FOR THE MAIN STAGE OF A CLASS-E_M AMPLIFIER

Circuit element	Formula
Total shunt capacitance of the switch	$C = C_\infty = \frac{3}{128}\frac{P_{OUT}}{V_{DC}^2 f_1}$
Power supply dc	$I_0 = \frac{3}{4}\frac{P_{OUT}}{V_{DC}}$
Load resistance (fundamental frequency)	$R_L = \frac{128}{9\pi^2}\frac{V_{DC}^2}{P_{OUT}}$
Load reactance[a]	$X_L = \frac{32(3\pi^2-32)}{9\pi^3}\frac{V_{DC}^2}{P_{OUT}}$
Injection-port component (2nd harmonic)	$R_{inj} = \frac{128}{9(\pi^2+16)}\frac{V_{DC}^2}{P_{OUT}}$
Injection-port reactance (2nd harmonic)	$X_{inj} = -\frac{16(3\pi^2+16)}{9\pi(\pi^2+16)}\frac{V_{DC}^2}{P_{OUT}}$

Infinite Q, 50% duty ratio and second-harmonic injection.

[a]Combination of C_{ser} and L_{ser} at f_1 with infinite loaded Q.

V. EXPERIMENTAL AND SIMULATION RESULTS

The authors wanted to verify the concepts and theoretical analyses given above, as follows.

1) Design a class-E [3] UHF power amplifier.
2) Build two identical amplifiers of that design and verify that they work properly.
3) Verify by testing that the two amplifiers have essentially identical electrical performance.
4) Change one of the amplifiers to class-E_M by adding the second-harmonic injection amplifier and its signal source, as described earlier in this paper.
5) Verify that this class-E_M amplifier works properly.
6) Test the class-E and -E_M amplifiers for output power, drain efficiency, and PAE (including the power consumption and efficiency of the added circuits in the class-E_M amplifier) as functions of the turn-on and turn-off switching transition times (with turn-on and turn-off set to the same transition time because almost all gate–drive circuits provide equal turn-on and turn-off transition times).
7) Plot the results.
8) Compare the measured results with predictions from the theoretical equations and draw conclusions.

Regrettably, limitations on funding and available labor time prevented our being able to accomplish the preceding list of tasks. We had to choose between no verification at all (undesirable) and the verification that we could afford to do: 1) laboratory tests of a full-power scaled-frequency class-E_M amplifier (13.2-W output at 3.5 MHz) and simulation of its main stage to verify that an actual amplifier does, in fact, operate in accor-

dance with the theoretical concepts developed in the preceding sections of this paper and 2) simulation combined with efficiency estimation of the 870-MHz class-E and class-E_M amplifiers that we were unable to build and test to verify that the type of operation predicted by the theory and observed at 3.5 MHz probably could also be obtained at UHF. We chose to do the preceding feasible verification rather than no verification at all. The procedures and the results are described below.

A. Experimental and Simulation Results at 3.5 MHz, 13.2 W

Fig. 4 shows the schematic of the experimental circuit simulated, built, and tested to verify the operation of the biharmonic class-E_M circuit with second-harmonic power injection ($n = 2$). To reduce the influence of parasitic wiring inductances, and to allow accurate time-domain measurements of the nonsinusoidal waveforms with the available instruments and low-cost transistors [International Rectifier IRFZ24N silicon power MOSFET: $V_{(BR)DSS} \geq 55$ V, $R_{DS(ON)} = 0.07\ \Omega$ max. @ ($T_j = 25\,^{\circ}$C, $I_D = 10$ A, and $V_{GS} = 10$ V)], the operating frequency was scaled down from microwave to 3.5 MHz. The loaded-Q values for the resonators at the outputs of the main stage ($C_{\rm ser}$ and $L_{\rm ser}$, loaded by their equivalent series resistances (ESRs) and R_L) and the auxiliary stage ($L_{\rm inj}$ and $C_{\rm inj}$, loaded by their ESRs and the impedance to ground at the output port of the main-stage transistor) were set to the unusually high values of approximately ten to obtain nearly sinusoidal currents in those resonators. That made the experimental circuit correspond accurately to the sinusoidal-currents assumption that was made to greatly simplify the theoretical analysis. Making the circuit operation correspond to the mathematical assumptions helps to ensure that comparisons between theory and experiment will be valid. A side effect of the high loaded Q's was power losses in the resonators being approximately 3.3 times as large as they would have been with the more-usual loaded-Q value of approximately three. That was not a serious problem: the circuit operation was not disrupted, and the increased losses could easily be accounted for, as is done in Table II. The resulting value of $L_{\rm ser}$ is

$$L_{\rm ser} = \frac{Q_{\rm loaded} R_L}{2\pi f_1} k \tag{32}$$

where k is a correction factor for considering the effect of parasitic series resistance of the output network that can be taken in the experimental setup as $k \approx (R_L + R_{\rm ser})/R_L = 1.07$.

The series-resonant circuit was tuned slightly off resonance so that the resulting reactance of the series circuit $X_{L\rm ser} + X_{C\rm ser} = X$ is equal to the reactance component of the load impedance Z_1 as seen in fourth row of Table I. In the experimental setup, $L_{\rm ser}$ was a fixed high-Q solenoid and $C_{\rm ser}$ was a variable capacitor with air dielectric. Similar considerations apply when calculating circuit elements of the injection generator. The injection generator must be designed for a load equal to the impedance components in rows 5 and 6 of Table I, and reactances of $C_{\rm inj}$ and $L_{\rm inj}$ to provide high-enough loaded quality factor (e.g., ten) at $2f_1$ for the theory to be applicable (considering only a limited number of harmonic components).

TABLE II
PARAMETERS OF THE MAIN STAGE OF THE INVESTIGATED 3.5-MHz CLASS-E_M AMPLIFIER

Parameters of the main stage	Simulated	Measured	Theory
DC supply voltage	11.5 V	11.5 V	11.47 V
Switch peak current (ref. Class E)	3.37 A	3.30 A[a]	3.25 A (3.28 A)
Switch peak voltage (reference Class E)	51.10 V	50.63 V	48.98 V (40.86 V)
Load resistance + + L_{ser} parasitic resistance	13.5 Ω +0.9 Ω	13.5 Ω +0.9 Ω	13.5 Ω +0.9 Ω
DC main input power	10.10 W	10.34 W	9.87 W
Injected power	3.93 W	4.40 W	3.29 W
Gate-driving power	54.11 mW	23.5 mW	0
Output power	12.98 W	13.23 W	12.34 W
L_{ser} finite-Q loss	0.87 W	1.01 W	0.82 W
PAE_{main_stage} [%] $\frac{P_{out} - P_{drive\_main} - P_{inj}}{P_{DC\_main}}$	89.1%	85.2%	91.7%
PAE adjusted for L_{ser} finite-Q loss [%] $\frac{P_{OUT} + P_{Lser} - P_{drive\_main} - P_{inj}}{P_{DC\ main}}$	97.6%	94.9%	100%
Total efficiency of the main stage $\frac{P_{OUT}}{P_{DC\ main} + P_{drive\ main} + P_{inj}}$	92.2%	89.6%	93.8%
Injected-power ratio $\frac{P_{inj}}{P_{inj} + P_{DC\ main}}$	28.0%	29.9%	25.0%
Power gain $\frac{P_{OUT}}{P_{drive\ main}}$	23.8 dB	27.5 dB	–
Total losses other than L_{ser} finite-Q loss (% of total input power)	1.7%	3.6%	0%

Reference Class-E values, shown in parentheses, are for Fig. 5(a).
[a]Determined indirectly from the measured waveforms as the value of the sum of the currents in L_{inj}, RF choke, and L_{ser} during the transistor "on" interval.

In the experimental setup, $C_{\rm inj}$ and $L_{\rm inj}$ were just chosen to provide high loaded Q without considering exactly the second-harmonic impedance of Table I. Instead of fine tuning $C_{\rm inj}$ or $L_{\rm inj}$, the main stage was tuned to continuous waveforms by initially tuning both $L_{\rm ser}$–$C_{\rm ser}$ and $C_{\rm inj}$–$L_{\rm inj}$ to resonance (the latter tuned to second harmonic) with high Q, and fine tuning in the second step the *phase* and *amplitude* (dc power supply) of the injection generator along with fine tuning of the capacitance $C_{\rm ser}$ until waveforms of the main stage approached those calculated theoretically [see Figs. 5(b) and 6(a)]. With limited resources, the authors did not perform optimum-efficiency tuning of the injection generator; the operation of the main stage and its correspondence to the derived theory were the main focus of their effort. We measured the output power of the injection generator, but not its dc input power or drive power. The method presented above, allowed us to focus on: 1) verifying that continuous voltage and current waveforms can be achieved at the main-stage transistor in accordance with the derived theory; 2) verifying of the theoretical harmonic-power relationships; and 3) considering efficiency issues related to switching in the main stage. The experimental observations and the theoretical predictions agreed well, and are summarized in Table II.

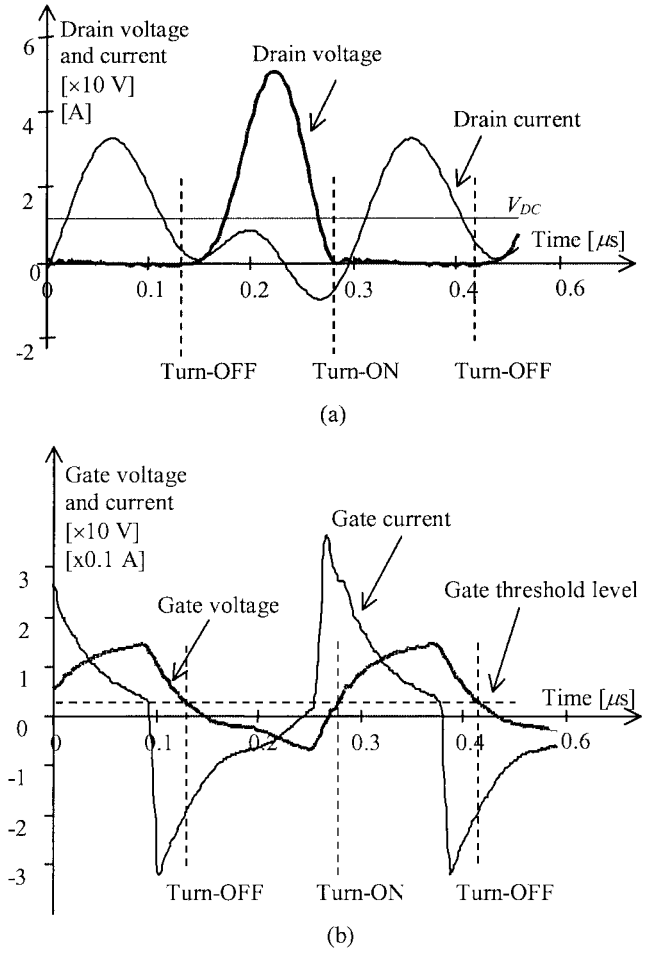

Fig. 6. Experimental current and voltage waveforms in the 3.5-MHz class-E_M amplifier (main stage). (a) Drain voltage and current. (b) Gate voltage and current.

Table II (see also Fig. 6 and comments below) summarizes measured results and the corresponding values predicted by simulation and theoretical analysis. (The theoretical circuit used for comparison in Table II is based on the theory presented in this paper: infinite-Q load networks to obtain pure-sine currents in L_{ser}–C_{ser} and in L_{inj}–C_{inj} to simplify the theoretical analysis. The only source of loss considered for the theoretical circuit in Table II is the parasitic series resistance of L_{ser}, set equal to the value measured in the experimental amplifier. For the SPICE-simulated class-E_M amplifier of Fig. 4, all capacitors and inductors, except L_{ser} and L_{inj}, were taken as lossless; L_{ser} and L_{inj} were given the values of ESR measured in the experimental amplifier. The transistor model was a complete SPICE model with parameter values provided by the software vendor.)

The peak transistor currents in a class-E_M main stage and a class-E output stage, using the same dc supply voltage and delivering the same output power to the load, are about equal. The peak transistor voltage in the E_M main stage is approximately 20% higher than that of a nominal class-E amplifier. The measured RF output power was 13.2 W and the measured PAE of the main stage was 85.2%. (The equation in Table II for main-stage PAE is adapted from the usual equation by also including the injected power that comes from the auxiliary stage.)

Parasitic losses in the output network (primarily in the ESR of L_{inj}) are not caused by switching transitions; therefore, the

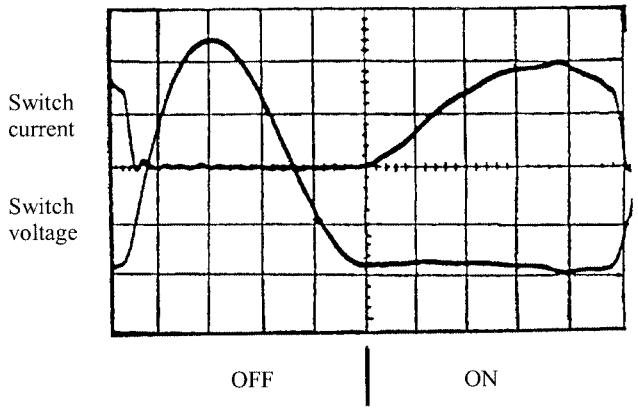

Fig. 7. Measured transistor voltage and current waveforms in a class-E amplifier from a previous project.

class-E_M concept (aimed at reducing switching losses) does not reduce those parasitic-ESR losses. To show the switching-loss effects more clearly, Table II provides a separate value of PAE adjusted for the effect of the finite-Q loss. The high adjusted value of $PAE_{\text{adj}} = 94.9\%$ shows very low switching losses. PSPICE simulations agreed well with the experimental results, giving confidence in the accuracy of the measurements.

All the measurement results agree well with theory and simulation, except that the theoretical values of the parasitic power losses in the circuit's parasitic resistances include only the loss in the inductor L_{ser}; the other losses are not yet included in the theoretical analysis. For example, the injected power at $2f_1$ necessary to achieve jumpless waveforms (injected-power ratio) was measured as 29.8% of the total input power to the main amplifier versus the theoretical value of 25%. The difference can be attributed to: 1) the power losses in the parasitic resistances of the components that were not yet included in the theoretical analysis: 2) harmonic power flow at the output port and the injection port of the class-E_M amplifier, of harmonic currents of orders *other* than the desired f_1 and $2f_1$ (a second-order effect not included in the theoretical analysis); and 3) harmonic power conversion in the nonlinear parasitic capacitances of the MOSFET. (The harmonic currents of orders other than f_1 and $2f_1$ result from the finite impedances of L_{ser} and L_{inj} at frequencies other than f_1 and $2f_1$.)

Fig. 6 shows the measured drain and gate voltage and current waveforms at the transistor of the main stage. The switching moments are marked with vertical dashed lines. The drain–current and drain–voltage waveforms of Fig. 6(a) are in accordance with the theoretical class-E_M waveforms in Fig. 5(b) and differ from the theoretical class-E waveforms in Fig. 5(a) and the measured class-E waveforms in Fig. 7. The "drain current" curve of Fig. 6(a) has a zero-crossing near the turn-on moment, and has a local minimum, approaching zero, near the turn-off moment, in accordance with the theoretical curve of Fig. 5(b). (The "drain current" curve includes the MOSFET active current (what we want to see) *plus* the capacitive currents in the MOSFET's output capacitance and the external shunt capacitor (a side effect of measurement limitations). This current was measured indirectly by summing the measured load current, the measured injection current, and the dc-supply current. The

MOSFET active current is zero during the "off" interval, not visible in Fig. 6(a), as it is in the theoretical curve of Fig. 5(b).)

Conclusion from these experimental measurements. The jumpless waveforms of the class-E_M concept *are* achieved with the biharmonic circuit (using $n = 2$), as expected. Those waveforms *do* result in very low switching losses, as expected. Both the SPICE simulation and experimental measurements show good quantitative agreement with the theoretical predictions.

B. Simulation Results at 870 MHz, 3.2 W

Simplified efficiency estimation of a 870-MHz class-E_M amplifier was done using the HEPA-PLUS simulation and computer-aided design (CAD) program from Design Automation Inc., Lexington, MA. The purpose was to compare the predicted performance of a class-E_M main stage with a class-E design using a transistor of the same technology, operating at the same fundamental frequency. Electrical parameters of an experimental 3.2-W E-pseudomorphic high electron-mobility transistor (E-pHEMT) with 0.5-μm gate length and 50-mm periphery produced by Alpha Industries Inc. (now Skyworks Solutions Inc.), Woburn, MA, were used during the simulations ($R_{DS(ON)} = 0.071\ \Omega$; $C_{OUT} = 14.1$ pF, also noted as C_{oss} in Fig. 4; series resistance of C_{OUT} equal to 0.1 Ω). For PAE calculation, it was assumed that transistor parameters (including the gate periphery) and parameters of the external circuit elements can be scaled proportionally in order to increase or decrease powers without affecting power ratios relevant to efficiency calculation. Simulations assumed linear variation of switch current with time, during the switching transitions. Turn-off and turn-on transition times were taken as being equal, as is usually the case in switching-mode power amplifiers.

Starting from a reference class-E design at 870 MHz, simulated by HEPA-PLUS, the optimum PAE of a reference class-E amplifier was calculated as a function of the switching times of the transistor. The optimization included the gate periphery, in addition to the circuit R, L, and C values. The class-E curve in Fig. 8 shows the result of the optimum PAE as a function of the switching times in percentage of the 870-MHz period. (The optimum gate periphery with this transistor varies from 47.1 to 59.3 mm for switching times from 0% to 27.5% of the period of 870 MHz.) For calculation of efficiency, power gain of the reference amplifier was taken as 12 dB at 5% switching times and $P_{drive} \sim 1/\text{sw\_time}^2$.

On the other hand, for the class-E_M, two stages must be considered and related power to be calculated. The E_M main stage operates at 870 MHz at 3/4 of 3.2-W output (assuming $n = 2$); the auxiliary stage is an optimized class-E circuit that delivers 1/4 of 3.2 W at 1740 MHz. Assuming that the auxiliary stage uses the same kind of transistor as in the main stage, except for having a smaller periphery as appropriate to a power level smaller than in the main stage by a factor of three, similar optimizations were performed for the injection amplifier as for the reference class-E, but at double frequency. (The optimum gate periphery varied from 12.5 to 14.6 mm for switching times from 0% to 27.5% of the period of 1740 MHz.) For the class-E_M auxiliary stage, *switching time* is the percentage of the period of 1740 MHz, and power gain is taken as 6 dB at 5% switching time; $P_{drive} \sim 1/\text{sw\_time}^2$.

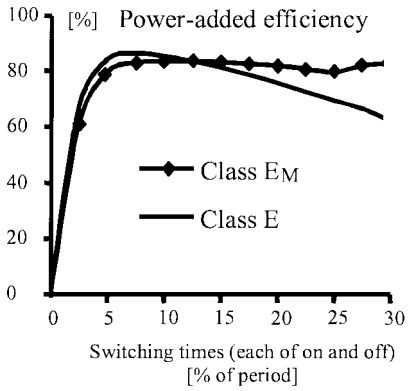

Fig. 8. PAE. Comparison of simulated class-E and class-E_M amplifiers delivering 3.2 W at 870 MHz. "Switching times" are the turn-on transition time and the turn-off transition time, each in percentage of the RF period of the signal in the amplifier, of the class-E amplifier and the class-E_M amplifier's main stage and auxiliary stage.

Without a dedicated optimization tool for class-E_M, power optimization of the auxiliary stage was not possible. However, for the E_M main stage (870 MHz), the switching transitions are essentially lossless, even at light input drive, because of the jumpless shapes of the voltage and current waveforms (see Section IV). Power gain of the lightly driven main stage was taken as 17 dB and drain efficiency of the E_M main stage was taken as equal to the drain efficiency of a simulated "equivalent" class-E amplifier that operates with fixed 1% switching times.

Fig. 8 shows the predicted PAEs of the class-E_M and class-E amplifiers as functions of the transistor switching times. (PAE for the class-E_M main stage is defined in this paper as $(P_{OUT} - P_{gate\text{-}main} - P_{gate\text{-}aux})/(P_{DC\text{-}main} + P_{DC\text{-}aux})$.) The peak value of PAE for the class-E_M amplifier is 3.3% lower than the peak value for the classical class-E amplifier, but the class-E_M PAE varies by only $+-2\%$ for all switching times (hence, drive powers) from 6% to 30% of the period, whereas the class-E overall efficiency drops monotonically from its peak to 73.5% of its peak value for switching times of 30% of the period, i.e., the class-E_M overall efficiency is much less dependent on switching times (hence, on input-drive power) than is the class-E overall efficiency. Important for a comparison of the optimally tuned class-E_M and class-E amplifiers is to have an accurate relationship between the transistor's switching transition times and its input-drive power. The authors assumed that switching times in the class-E amplifier are inversely proportional to the input-drive current (hence, to the square root of the input-drive power).

Due to the fact that the class-E_M amplifier is able to divide the place of power conversion into a higher power subsystem operating at lower frequency and a lower power subsystem operating at a higher frequency, separation of the power-processing mechanisms allows using different technologies in the different stages (e.g., lower cost and higher power, but lower frequency main stage combined with higher cost and higher frequency, but lower power auxiliary stage). The simulation comparison focused on a simplified case with the same transistor technology being used in both transistors (same set of transistor parameters, with their numerical values scaled for different peripheries and power ratings). Optimizing the technologies *separately* for the two stages opens new possibilities for optimizing the overall design.

VI. New Results

Jumpless waveforms of switch current and voltage are desirable for obtaining high efficiency in switching-mode RF power amplifiers (such as the class-E amplifier [1]–[6]) operating at frequencies high enough that the achievable transistor switching times are longer than approximately 15% of the period. Another advantage is that operation with jumpless waveforms allows greatly reduced switching times (as compared with the same transistor and RF-input drive being used in a class-E amplifier [1]–[6]), which also yields reduced switching losses.

Previous work [11]–[13] showed that no output power can be obtained from a switching-mode power amplifier comprising linear passive components and an ideal switch if *both* the switch-voltage waveform *and* the switch-current waveform are jumpless and power flow on harmonics is unidirectional.

A new general equation (15), and its special case (16) for an amplifier with jumpless switch voltage *and* current waveforms were derived to characterize the operation of a lossless-mode amplifier comprising a linear or nonlinear load network driven by an ideal switch operating at the desired output frequency. These equations are useful in deriving mathematically the topologies of circuits that can yield high efficiency even if the transistor switching time is longer than the useful limit for the class-E amplifier of approximately 20% of the RF period. The power equation (23) helps in determining the power levels needed to generate jumpless switch-current and switch-voltage waveforms.

Reasoning from the new general equation (15), a feasible new topology is conceived, which can have jumpless switch-current *and* switch-voltage waveforms *and still deliver output power*. The topology is a modified version of the class-E power amplifier using *nonlinear* passive or active components and an ideal switch. The new version is called "class E_M"; the "M" subscript originally denoted "Microwave" because this technology is intended for use at frequencies high enough that the transistor turn-off transition time could not conveniently be made small enough to yield good efficiency in class-E operation. After the death of our coauthor Dr. B. Molnár, we interpret the "M" subscript as "Molnár" to honor and remember the inventor of the class-E_M concept.

- The theory of the new class-E_M amplifier is given.
- The switch voltage and current waveforms of the biharmonic (for $n = 2$) realization of the class-E_M amplifier are derived.
- Computer simulation and measurement results on a scaled-frequency 3.5-MHz 13.2-W prototype show that switching loss practically disappears when the switch is operated in the class-E_M regime.
- Theory, simulation, and measurements all agree well.

VII. Questions Needing Further Investigation

A. How Much Input Drive is Needed?

The low values of the transistor switching losses indicate that the main stage of the class-E_M amplifier can operate in a true switching mode, even with small input drive. Experimental results, and simulation of a class-E_M stage, show that the switching losses in the main stage practically disappear in the jumpless-waveforms operation. As a consequence, the gate-drive power can be reduced below what would be needed in a classical class-E amplifier, as far as switching losses are concerned. However (as a separate requirement), the input drive must be sufficient to yield a low saturation voltage while the transistor is conducting substantial current. Those two requirements are essentially separated from each other. If the input drive required for low saturation voltage would produce faster switching transitions than are needed for low switching losses, the designer has the option of choosing a slower switching transistor that could have a chosen combination of higher breakdown voltage, higher "ruggedness" in operation with high-standing-wave-ratio load, and lower cost. The choice of how much input drive to apply can be based almost entirely on the amount needed to operate the conducting transistor in deep-enough voltage saturation because switching losses will be almost eliminated by the class-E_M waveform shaping and, therefore, large drive is not needed to reduce switching losses. The optimum input drive is that which minimizes the *sum* of power dissipation at the transistor output port (decreases with increasing drive) and dc power consumption of the driver circuit (increases with increasing drive). A similar optimization procedure applies to the auxiliary stage, except there, the switching losses are not being reduced by the presence of jumpless waveforms.

B. Is the Benefit Obtained From the Jumpless Operation Worth the Additional Cost?

The costs of the improvements of the class-E_M amplifier with auxiliary injection generator over the classical class-E version are: 1) a harmonic-current generator must be added to supply (at $2f_1$) $1/2^2 = 1/4$ of the desired load power or to supply (at $3f_1$) $1/3^2 = 1/9$ of the desired load power, etc. [see (15)] and 2) the conduction losses might increase, depending on the input drive that is supplied (see Question A above).

The auxiliary stage has to supply its power with the correct phase and amplitude, which might make more difficult work for the designer. The theoretical value (with infinite Q) of the "Transistor Utilization Factor" $P_{\rm OUT}/V_{\rm peak}I_{\rm peak}$) of the main-stage transistor is approximately 20% lower than that of a device in a class-E design, but the practical values require further study. (For comparison of theoretical versus measured values of peak voltage and peak current, see columns 3 and 4 of Table II.) Offsetting those factors are: 1) the reduced losses during the switching transitions and 2) output and input powers of the driver stage for the main amplifier can be lower than for the conventional class-E amplifier of [1]–[3] because fast switching time of the main amplifier's transistor is now much less important.

C. Will the Auxiliary Amplifier Consume More Power Than the Reduction of Power Dissipation in the Main Amplifier?

"Yes," if the switching times in the main amplifier are *already* fast enough to result in low switching losses. However, if the switching losses are already low enough, there is no need to use the jumpless waveforms and the associated class-E_M technology; they should be used only if they are needed. However,

if the switching losses are large (as in the class-E amplifier in Fig. 9 at 30% switching times), the answer might be "No." This is more likely to be the case if the auxiliary amplifier uses a faster switching transistor than is used in the main amplifier, as discussed in the last paragraph of Section V-B.

D. However, if the Main Stage Switches Slowly, Won't an Auxiliary Stage Using the Same Transistor Technology, at Double the Frequency, Switch Even More Slowly (as a Percentage of the Period of the Signal It Is Producing)?

"Yes." Depending on the electrical parameters, the resulting amplifier efficiency might be lower or higher than that of a classical class-E amplifier. As one reviewer put it, "If the fundamental class-E amplifier is limited by slow transitions, a second or higher harmonic amplifier in the same technology may have more severe limitations." The use of a higher frequency transistor in the auxiliary stage than in the main stage increases the likelihood that the class-E_M amplifier will provide higher efficiency than a classical class-E amplifier. Until more-refined prediction methods become available, each case must be investigated according to its particular set of electrical parameters.

VIII. Comparison With Current–Source Class F and Harmonic-Control Amplifier (HCA) Linear RF Power Amplifiers

The class-E switching-mode power amplifier and its class-E_M derivative provide high efficiency because the power transistor is operated as a switch: fully on (operating in deep voltage saturation) and fully off, with the transitions between those two states occupying as small a fraction of the RF period as feasible, and with the transistor voltage and current waveforms shaped to minimize the fraction of the period during which appreciable voltage and appreciable current exist simultaneously, thus minimizing the $v \cdot i$ product, which is transistor power dissipation. Reference [3] gives a detailed description of class-E circuit operation; the class-E_M derivative (described in this paper) further improves the reduction of power dissipation during the switching transitions. The input drive to the power transistor is intended to be full drive when the amplifier is supposed to produce output power, and no drive when the amplifier is not to produce output power. The design makes no provision for partial input drive and partial output, as would be used in a *linear* amplifier that provides a *linear* input–output amplitude transfer function. The switching-mode amplifiers are hard-limiting amplifiers. Fig. 9 illustrates conceptual amplitude input–output transfer functions for: 1) a linear amplifier, such as class F [15] and HCA [16], [17] and 2) a switching-mode amplifier, such as classes E and E_M. The hard-limiting transfer function of 2) is suitable for continuous-wave and on/off applications, e.g., RF power generators, FM transmitters, and pulsed transmitters producing binary-coded or pulsewidth-modulated signals. That amplitude transfer function is *not* suitable for a *linear* RF power amplifier, in which envelope modulation of the input signal is intended to be reproduced linearly in the output signal, unless the hard-limiting amplifier is *augmented* with an amplitude-control subsystem, as in the envelope

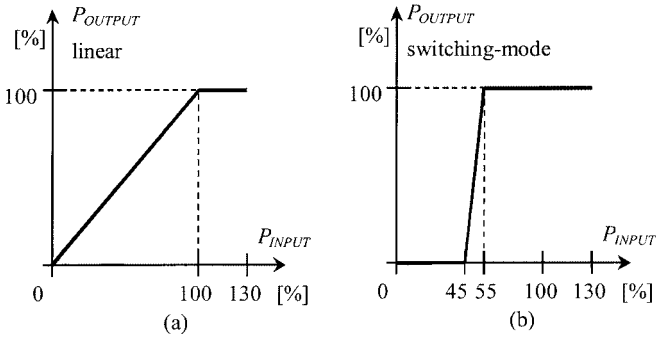

Fig. 9. Idealized input–output characteristics of power amplifiers. (a) Linear amplifier. (b) Switching-mode amplifier.

elimination and restoration (EER) system [18]. For that reason, a class-E or -E_M amplifier, *without* an added amplitude-control subsystem, is not appropriate for amplifying simultaneous multiple signals, and intermodulation distortion is not a relevant amplifier-evaluation factor. If the span of the transition region of the transfer function 2) is intentionally made large, to try to operate the amplifier as a linear power amplifier, we would have an amplifier whose load network was designed to generate high-efficiency voltage and current waveforms when driven at its input port by a *periodically operated switch*, but which is being driven only partially, by a transistor that is *not* operating as an on/off switch, but is operating as a pulsed current source. *A priori*, one would not expect superlative performance from a circuit that is not being operated in the way it was designed to operate. These remarks about the class-E and class-E_M amplifiers apply also to the class-D amplifier [19], another type of switching-mode power amplifier in which the transistors operate as switches. (Reference [19] describes a high-efficiency switching-mode oscillator circuit, but the circuit was quickly adapted to power amplifiers.)

If a power amplifier with a *linear* input–output amplitude transfer function is required, the proper choice is an amplifier in which the power transistor operates as a controlled-amplitude current source, *not operated in deep voltage saturation*. Thus, the collector–emitter or drain–source voltage will always be large enough to keep the transistor in current saturation, i.e., of the order of a few volts, depending on the transistor characteristics and the amount of current required. Such an amplifier *must* have lower efficiency than a switching-mode amplifier, which operates the "on" transistor in voltage saturation, at a voltage of the order of a few tenths of a volt, $R_{DS(ON)}$ or $R_{CE(sat)}$ times the required current; the next paragraph gives a numerical example. The efficiency of the current–source amplifier can be improved by shaping the current waveform and/or the load-network input-port impedance such that the transistor–voltage waveform approximates a flat bottom rather than the bottom of a sine-wave during the time that the transistor is conducting appreciable current [15]. That flat-bottom voltage waveform results in less power dissipation in the transistor during the time that the transistor is conducting current, thus increasing the efficiency. That type of amplifier was called "biharmonic" by Russian authors or "polyharmonic" by Bulgarian authors; the bibliography of [1] contains references to those amplifiers. Since about the 1990s, those amplifiers have usually been referred to

as class F; the HCA [16], [17] is in the class-F family. An unfortunate source of confusion is that two other types of amplifiers that operate their transistors as *switches* (*not as current sources*) have *also* been referred to as "class F"; they have no relation to the current–source linear amplifiers discussed here.

The efficiencies of a linear amplifier at full output and a switching-mode amplifier can be compared as follows using simplified models for illustration of the concepts. Let us assume, for simplicity, that both amplifiers operate with rectangular voltage and current waveforms. In both amplifiers, the current waveforms have minimum values of zero. The linear amplifier operates the transistor in current saturation, at a voltage of $V_{\min(\mathrm{lin})}$ when the transistor is conducting current. The switching-mode amplifier operates the transistor in deep voltage saturation when conducting current, at a voltage of $V_{\min(\mathrm{sw})}$ when the transistor is conducting current. Both amplifiers operate from a collector/drain supply voltage of V_{DC}. The collector/drain efficiency of the linear amplifier is $[1 - V_{\min(\mathrm{lin})}/V_{\mathrm{DC}}]$. The collector/drain efficiency of the switching-mode amplifier is $[1 - V_{\min(\mathrm{sw})}/V_{\mathrm{DC}}]$. For a numerical example, use $V_{\mathrm{DC}} = 3.2$ V (typical for cellular-telephone handsets), $V_{\min(\mathrm{lin})} = 1$ V, and $V_{\min(\mathrm{sw})} = 0.5$ V. The efficiency of the linear amplifier will then be $[1 - (1\ \mathrm{V})/(3.2\ \mathrm{V})] = 68.8\%$ and the efficiency of the switching-mode amplifier will be $[1 - (0.5\ \mathrm{V})/(3.2\ \mathrm{V})] = 84.4\%$.

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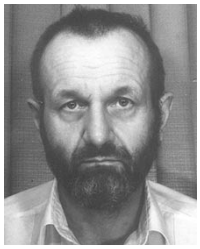

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